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The Fu Foundation School of Engineering and Applied Science

ELEN E3106/4106 Lecture 20

MOS Capacitor Part II

Outline

- PMOS vs NMOS
- PMOS band diagrams under biasing conditions
- C-V characteristics
- Non-idealities in the C-V curves
- CCD imager applications

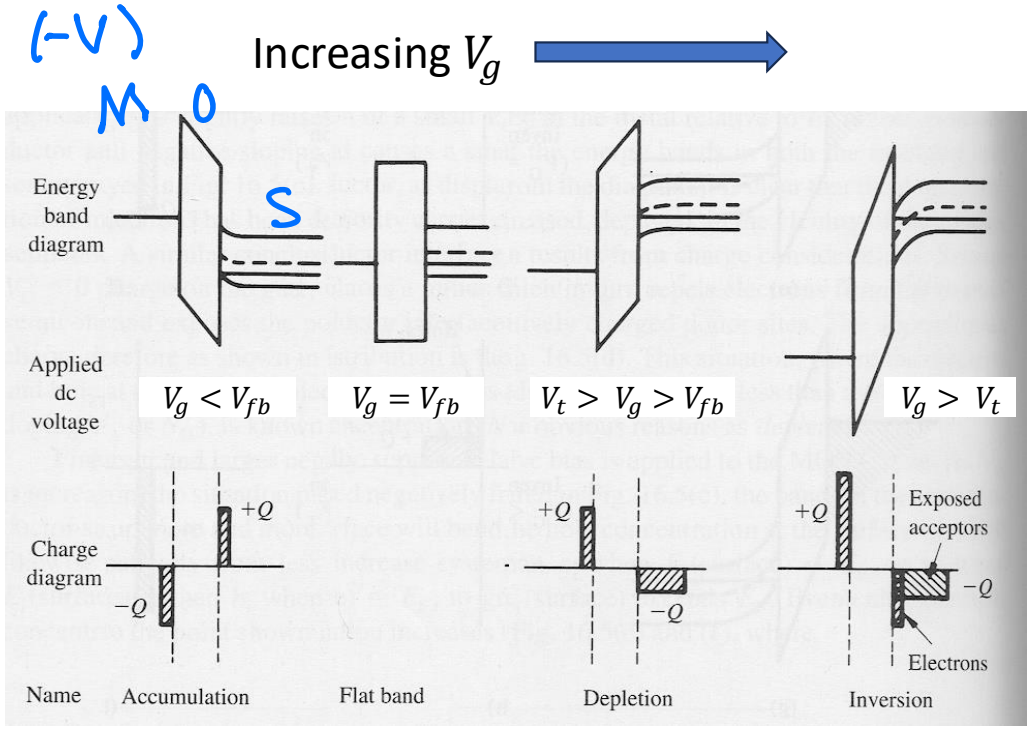
Assignments:

Reading: C. Hu §5.6,5.10.1

Homework 8 due Monday Dec. 1st by 11:59pm

Recap of MOS Capacitors So Far…

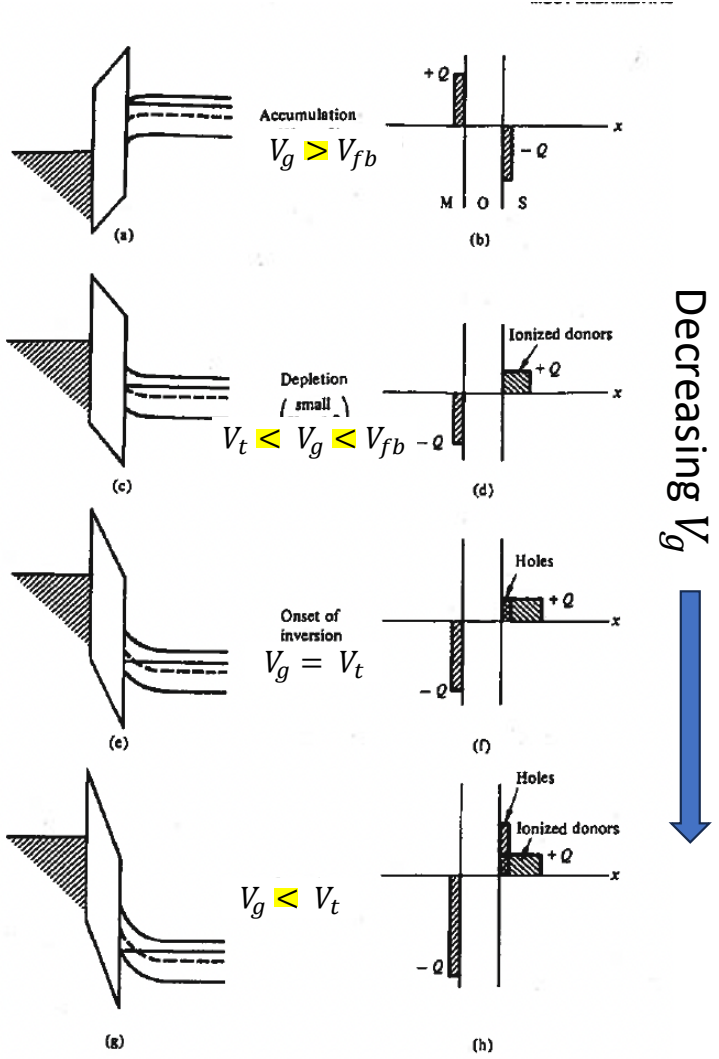
- We discussed different gate bias conditions
  - Accumulation
  - Flat-band
  - Depletion
  - Threshold
  - Inversion
- Note we have focused on NMOS (the inversion layer is made of e⁻) p-type bulk
- Recall: y-axis of band diagram represents energy of an e-
- Voltage corresponds to P.E. of *positive* charge, so reduces energy of e- and bends the bands downwards
- Assumption: No charge stored inside of oxide!



Sources: E. Pop ECE 340 Lecture Slides

PMOS Capacitor

- *n-type* semiconductor body with p-type inversion layer of holes at the surface
- Same gate bias conditions, but the sign on the gate is flipped
  - Accumulation: e- accumulate at surface
  - Flat-band: no E-field
  - Depletion: e- repelled from surface
  - Threshold: onset of inversion ($p_s =$ Nd)
  - Inversion: surface becomes p-type



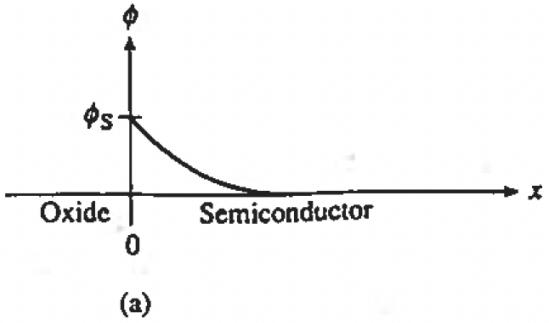
& magnet analogy
(+) V_g "attracts" e^-, (-) V_g "attracts" h^+

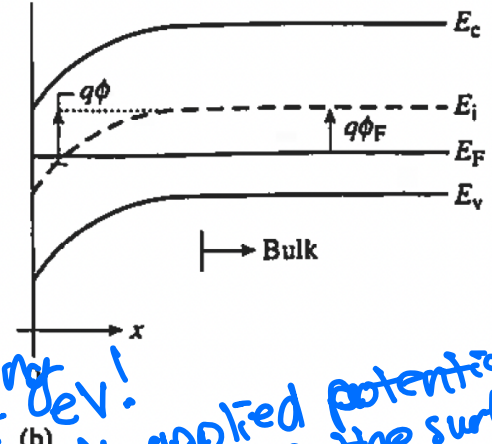
Sources: R. Pierret *Semiconductor Device Fundamentals*

Another look at Surface and Bulk Potential

- Let $\Phi(x)$ be the electrostatic potential inside the semiconductor at any point x
  - $\Phi(x) = \frac{1}{q}[E_i(bulk) - E_i(x)]$
- Let x = 0 at the oxide-semiconductor interface. The surface potential is:
  - $\Phi_s = \Phi(x = 0) = \frac{1}{q}[E_i(bulk) - E_i(surface)]$
- As x increases, the E-field goes to 0
- But what about Φ_F? Recall $\Phi_s = 2\Phi_F$ at the depletion-inversion threshold
  - $\Phi_F = \frac{1}{q}[E_i(bulk) - E_F]$
  - This is a material parameter! Since it depends on E_F, it depends on the doping
  - For p-type bulk (NMOS): $\Phi_F = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) > 0$
  - For n-type bulk (PMOS): $\Phi_F = \frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right) < 0$
- Why do we denote these potentials Φ instead of V?

Graphical definition of $\Phi(x)$, Φ_s (a). The relationship between $\Phi(x)$ and bending bending; graphical definition of Φ_F (b).





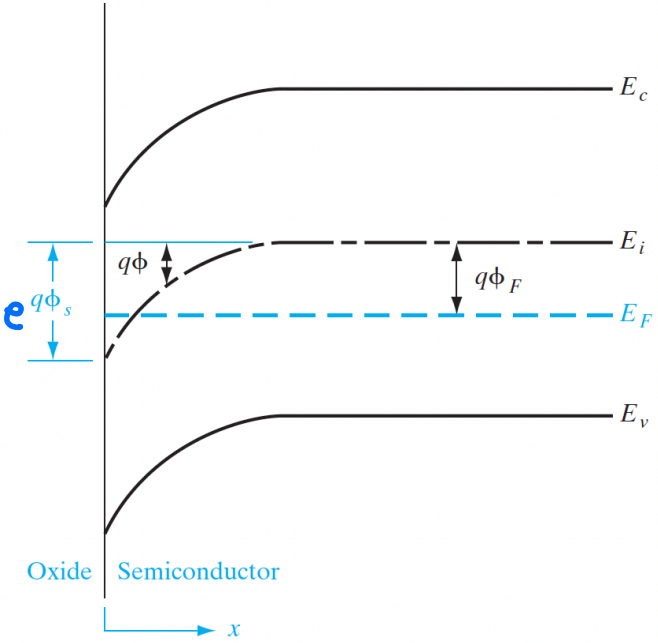
we are talking eV! No applied potential at the surface

Sources: R. Pierret *Semiconductor Device Fundamentals*

Weak vs. Strong Inversion in MOS caps

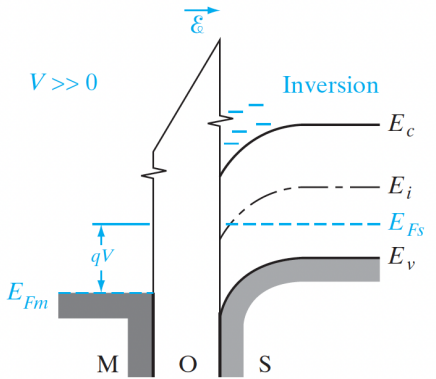
Weak Inversion

- Occurs when $\Phi_F < \Phi_S < 2\,\Phi_F$
- The intrinsic level Ei at the surface has just crossed below the Fermi level EF
- The surface is inverted in type (e.g., p-type substrate becomes weakly n-type), but the **inversion charge** is still small compared to the **depletion charge!**



Strong Inversion: $\phi_s(\text{inv.}) = 2\phi_F = 2\frac{kT}{q}\ln\frac{N_a}{n_i}$

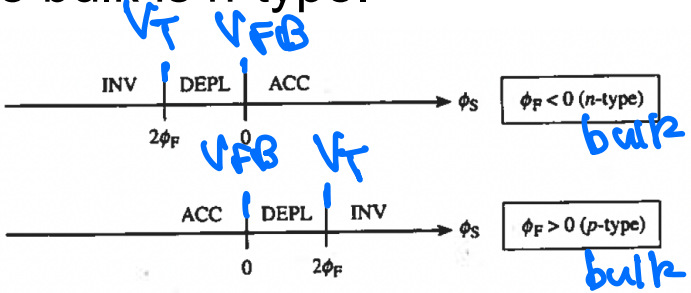
- Condition: The surface is **as strongly inverted** as the bulk is doped:
  $n_{surface} = p_{bulk}$ (surface electron density equals bulk hole density).
- The intrinsic level Ei at the surface lies as far **below** EF



Sources: R. Pierret *Semiconductor Device Fundamentals*

Energy Band Diagram Summary

- Energy band diagrams for the two dominant types of MOS caps shown here
- n-type (NMOS) devices have an n-type! inversion layer. The bulk is p-type.
  - $p_{bulk} \approx N_a$
- p-type (PMOS) devices have a p-type! inversion layer. The bulk is n-type.
  - $n_{bulk} \approx N_d$



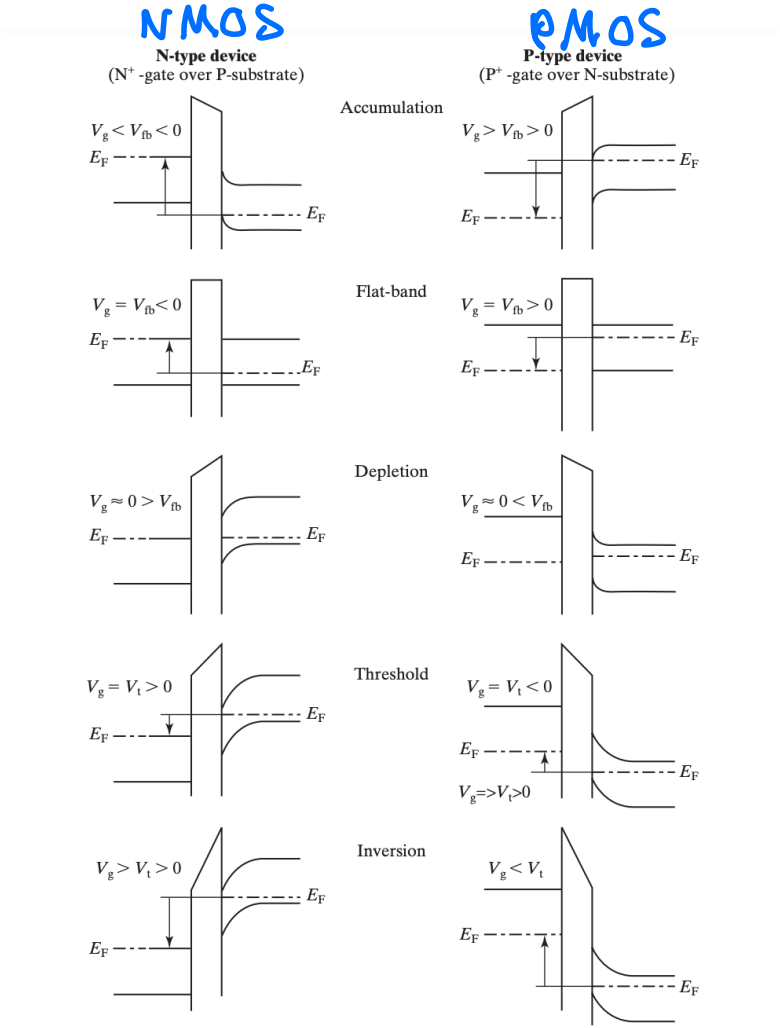
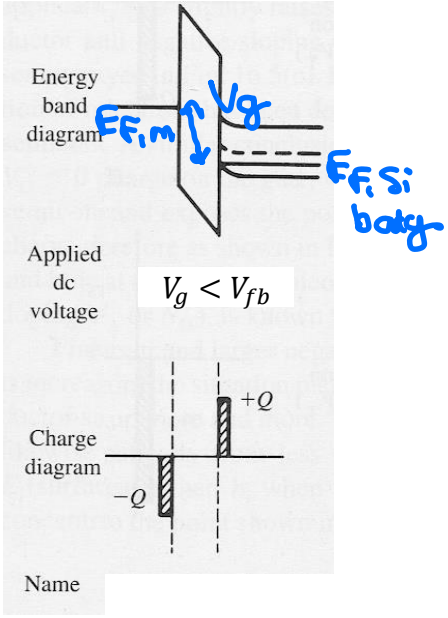


FIGURE 5–33 Energy band diagrams of the two dominant types of MOS capacitors. An N-type device is so named because it has N-type inversion charge that increases with a more positive V_g, and a P-type device has P-type inversion charge increasing with a more negative V_g.

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Guidelines for Drawing MOS Band Diagrams

- E_F is flat (constant with distance x) in the semiconductor bulk
  - Since no current flows, we assume equilibrium conditions hold
- Band bending is linear in the oxide ($\frac{dE_c}{dx}$ is const.)
  - No charge in oxide ($\frac{dE}{dx} = 0$) so E-field is constant
- The MOS "type" refers to the type of inversion layer
- As we've seen with every other device type, there's an equivalent p-type MOS cap to an n-type MOS cap
  - p^+-poly gate over n-type substrate
- The vertical distance between the Fermi level in the metal and the Fermi level in the Si body is equal to the applied gate voltage: $qV_g = E_{F,semi} - E_{F,m}$



Sources: R. Pierret *Semiconductor Device Fundamentals*

Problem: Calculating Flat-band and Threshold Voltages

Calculate the flat-band voltage of a silicon NMOS capacitor with substrate doping $N_a = 10^{17}\ cm^{-3}$ and an aluminum gate ($\Phi_M = 4.1\ V$). Assume there is no fixed charge in the oxide or at the oxide-silicon interface. Calculate the threshold voltage given a 20 nm thick oxide ($\epsilon_{ox} = 3.9\epsilon_0$).

$$V_{FB} = \Phi_M - \Phi_{semi} = \Phi_{MS} = \Phi_M - \chi - \frac{E_g}{2} - kT\ln\left(\frac{N_a}{n_i}\right)$$

$= \Phi_F$

$$= 4.1 - 4.05 - \frac{1.1}{2} - 0.026\ln\left(\frac{10^{17}}{1.5\times10^{10}}\right)$$

$= 0.408$

$$V_{FB} = -0.91\ V$$

$$V_T = V_{FB} + 2\Phi_F + \frac{\sqrt{qN_a 2\epsilon_{Si} 2\Phi_F}}{C_{ox}}$$

$$C_{ox} = \frac{\epsilon_{ox}}{T_{ox}}$$

$$= -0.91 + 2(0.408) + \sqrt{\frac{(1.6\times10^{-19})(10^{17})(2)(11.8)(0.408)(2)\epsilon_0}{(3.9)\epsilon_0/(20\times10^{-7}\,cm)}}$$

$$V_T = 0.96\ V$$

Sources: E. Pop ECE 340 Lecture Slides

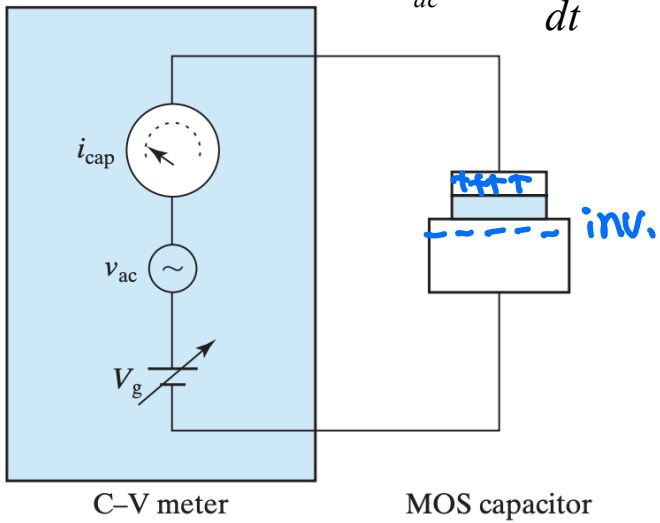
MOS C-V Measurement Setup

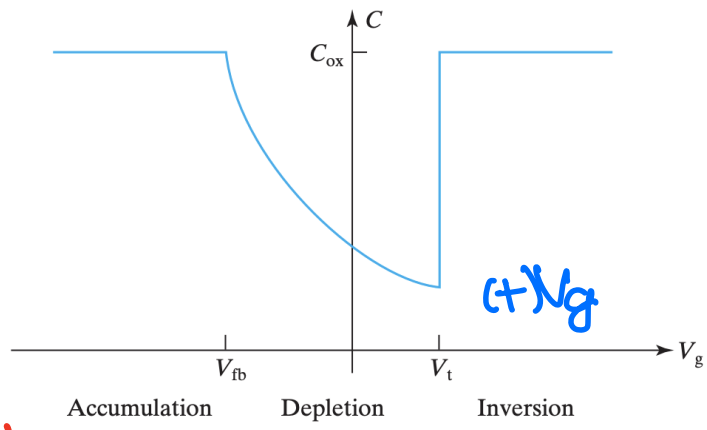
- Since this is a capacitor, what does the C-V curve look like?
- C-V characteriation is powerful and commonly used
- Useful to determine the oxide thickness, doping, V_T, V_{FB}
- Looking at the small-signal capacitance,

$$C \equiv \frac{dQ_g}{dV_g} = -\frac{dQ_{sub}}{dV_g}$$

- Recall: (-) sign is because V_g is applied at top plate but Q_{sub} is taken at bottom plate
- This C-V curve is idealized
- Question: is the substrate p-type or n-type? How do we tell? V_t is (+) → nMOS → p-type substrate

$$i_{ac} = C\frac{dv_{ac}}{dt}$$

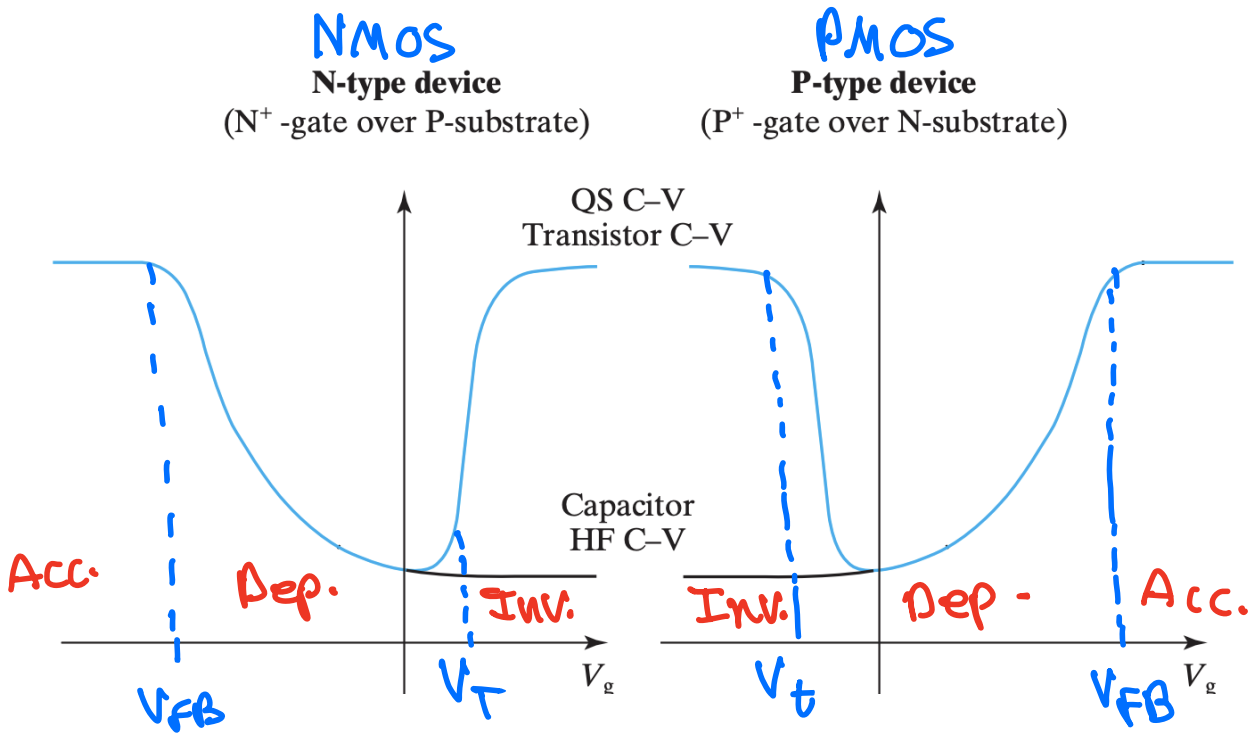




Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

MOS C-V Measurement Setup

- Recall our gate voltage conditions for different biasing!



- Which one is PMOS? How about NMOS? See above!

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Idealized MOS C-V Curve

- The capacitance is:

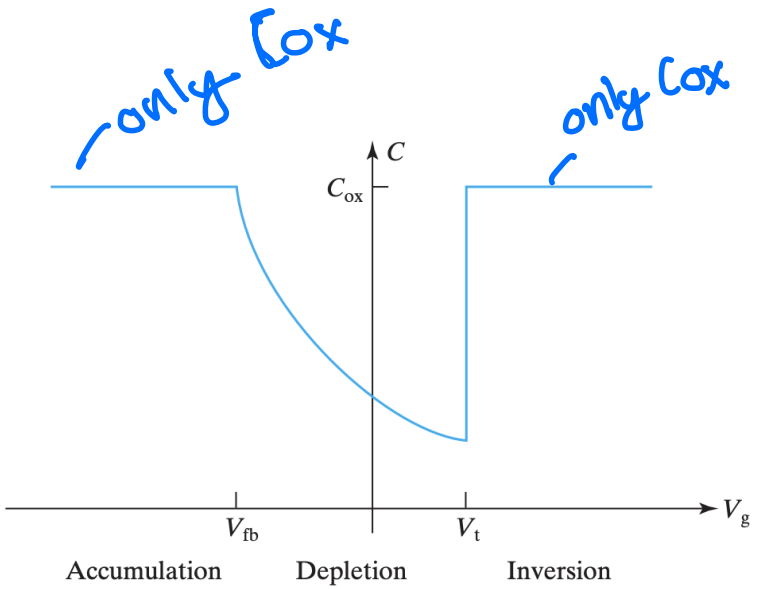
$$C_{dep} = \frac{\varepsilon_s}{W_{dep}}$$

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

- caps in series

$$\frac{1}{C} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_g - V_{fb})}{qN_a\varepsilon_s}}$$

- Where we have solved for W_{dep} in terms of V_g using our earlier relation:



$$V_g = V_{fb} + \phi_s + V_{ox} = V_{fb} + \frac{qN_aW_{dep}^2}{2\varepsilon_s} + \frac{qN_aW_{dep}}{C_{ox}}$$

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

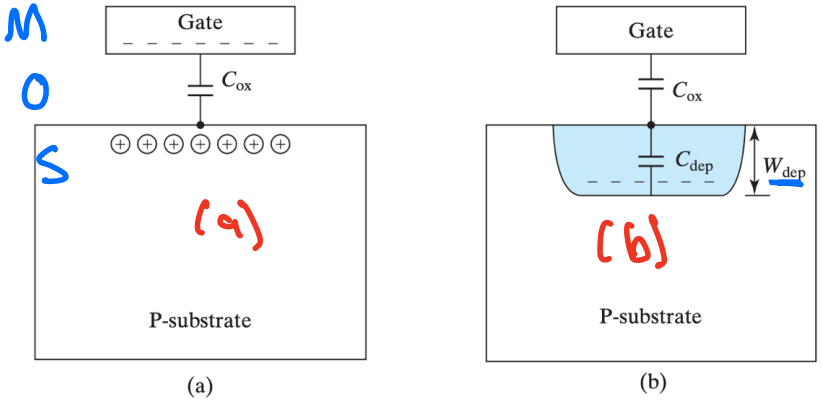
MOS C-V Curve: Accumulation and Depletion

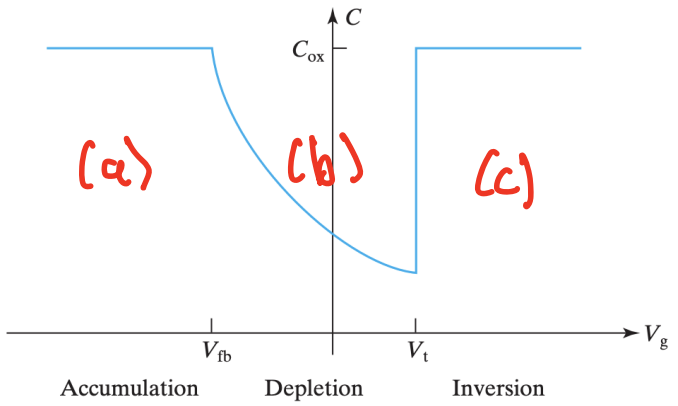
- Let's look at the curve from left to right (increasing V_g)
- Accumulation: there is no depletion region so C_{dep} = 0 and $C = C_{ox}$
- Depletion: Our equation above tells us that as V_g increases beyond V_{fb}, W_{dep} expand and therefore $C^{-1} = (C_{dep} + C_{ox})^{-1}$
- But why does $C = C_{ox}$ in the inversion region?

$$C_{\text{total}} = \left(\frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{inv}}}\right)^{-1} \approx C_{\text{ox}}$$

$C_{inv} \to \infty$, $\frac{1}{C_{inv}} \to 0$ (c)

(a) Accumulation region; (b) depletion region





Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

MOS C-V Curve: Inversion Cases

Inversion Case I: inversion layer minority carriers can be supplied quickly enough to respond to changes in V_g

- Called quasi-static (QS) C-V
- This case hold true at *low frequencies* (LF)

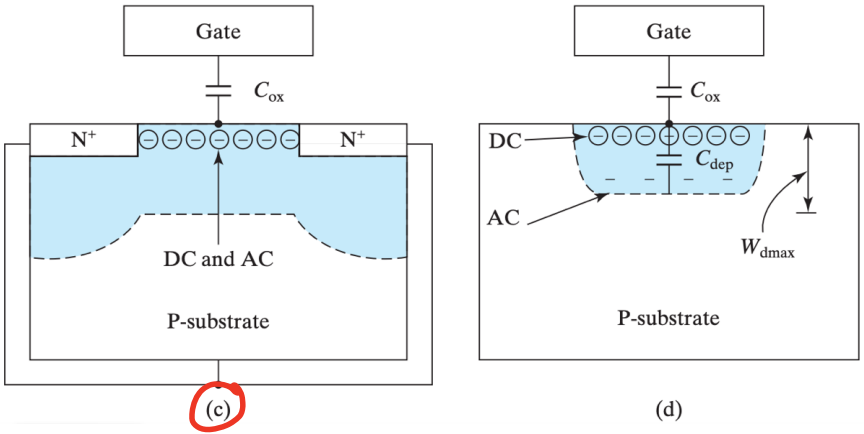
- How are they supplied?
  1. Optical generation Not applicable for MOS!
  2. Providing a nearby source of minority carriers like in a MOSFET

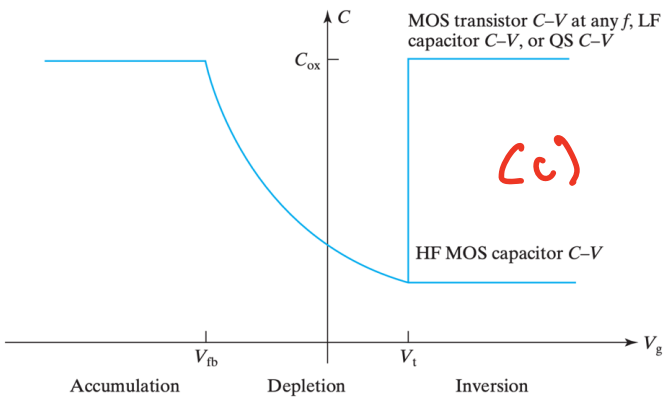
Inversion Case II: inversion layer charge Q_{inv} cannot be supplied quickly enough to respond to changes in V_g

- Thermal generation is slow!
- This case hold true at *high frequencies* (HF)
- Q_{inv} cannot respond to fast AC signal and remains constant at DC value
- W_{dep} will expand or contract slightly around W_{dmax} (relies on majority carriers). So AC charge exists at the bottom of dep. reg.

- This means our C-V curve looks different depending on the gate voltage frequency: HF, or LF/QS

(c) inversion region with efficient supply of e- from the n+ regions in a MOSFET; (d) inversion region with no or weak supply of inversion e-





Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

C-V of MOS Capacitor vs MOSFET

- What values are considered “high” or ”low” frequency?
- Depends on device type!
  - E.g. whether we have an efficient source of minority carriers
- MOSFETs (transistors) remain QS up to higher frequencies than MOS Caps
- In other words, MOS Caps will enter inversion case II at lower frequencies than MOSFETs

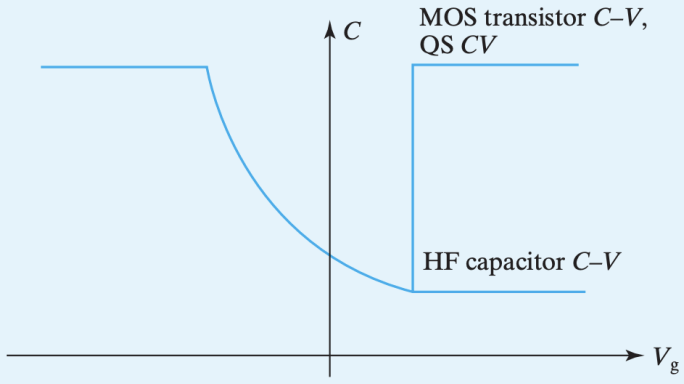


FIGURE 5–19 *C–V* curves of MOS capacitor and transistor.

For each of the following cases, does the QS *C–V* or the HF capacitor *C–V* apply?

(1) MOS transistor, 10 kHz. (Answer: QS *C–V*).
(2) MOS transistor, 100 MHz. (Answer: QS *C–V*).
(3) MOS capacitor, 100 MHz. (Answer: HF capacitor *C–V*).
(4) MOS capacitor, 10 kHz. (Answer: HF capacitor *C–V*).
(5) MOS capacitor, slow V_g ramp. (Answer: QS *C–V*).
(6) MOS transistor, slow V_g ramp. (Answer: QS *C–V*).

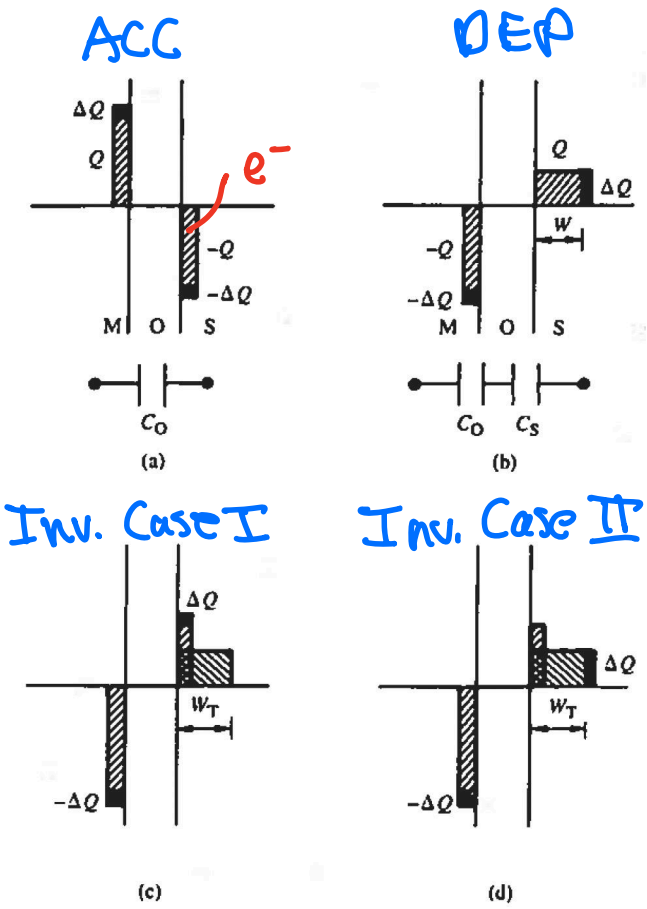
Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Charge Fluctuations under AC Conditions

- Note: C_{ox} is the being added or subtracted close to the edges of the insulator
- Black shaded regions represent ΔQ, change in charge from AC signal
- Accumulation: pile-up of e-. majority carrier driven process! State of system can be changed rapidly
- Depletion: dep. layer charge from withdrawal of majority carriers from W_{dep}

  Once again – majority carrier process! W_{dep} can fluctuate almost instantaneously
- Inversion Case I: Minority carriers are piled up at the interface. As $\omega \rightarrow$ 0, minority carriers CAN be generated or annihilated in response to AC signal
  - Charge is added or subtracted close to interface in inversion layer.
- Inversion Case II: As $\omega \rightarrow$ ∞, sluggish minority carrier R/G processes CANNOT supply/eliminate minority carriers in response to AC signal
  - # of carriers in inversion layer therefore remains fixed at DC value. Depletion region charge fluctuates around $W_{d,max}$
  - Because $W_{d,max}$ is independent of DC V_g, our HF C-V curve is also flat in inversion case 2 but lower than in case 1 since we have the equivalent of 2 parallel plate caps now

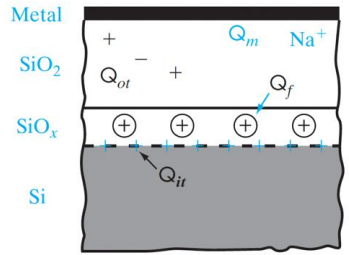
(a) Accumulation, (b) depletion, (c) inversion at low frequency, (d) inversion at high frequency



Sources: R. Pierret *Semiconductor Device Fundamentals*

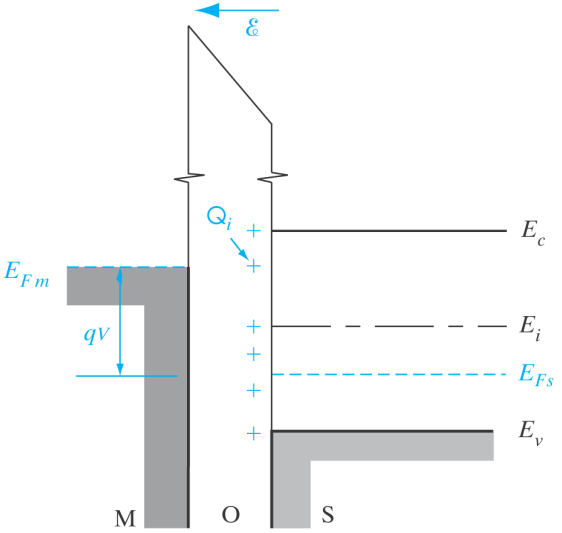
MOS Cap Non-Idealities

- The insulator (dielectric) and O-S interface are not atomically perfect
  - Mobile ions
  - Dangling bonds
  - Charge trapped within SiO_2
- How do we account for these charges?
- We can group them together as an equivalent sheet of charge $Q_i > 0$ at the O-S interface
- The (+) charge bends the E-bands at the interface and changes the field across the insulator!
- This shifts the flat band voltage: $V_{fb} = \Phi_{ms} - Q_i/C_{ox}$
- This interface charge is why $V_g = V_{fb} \neq 0$ in reality!



Q_m Mobile ionic charge
Q_{ot} Oxide trapped charge
Q_f Oxide fixed charge
Q_{it} Interface trap charge

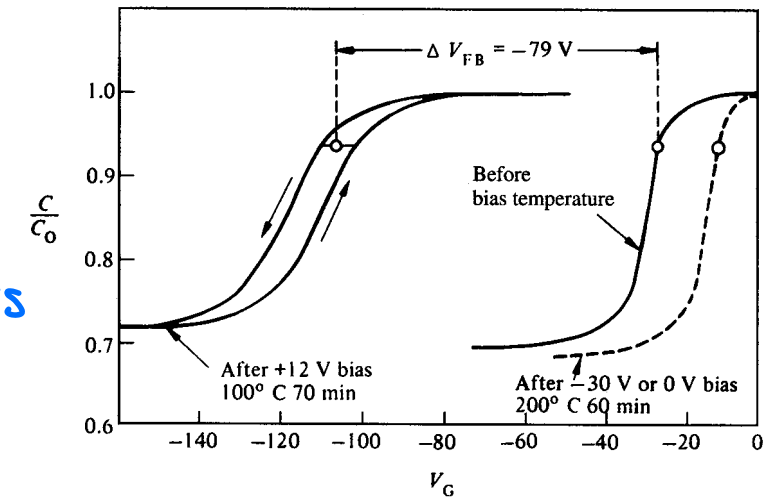
(a)



Sources: Textbook

MOS Cap Non-Idealities

- Odd shifts with temperature and bias in the measured C-V characteristics were once a mystery
- Source of the problem: mobile ionic charges (e.g. Na+, K+) moving to/away from interface
  - $\Delta V_{fb} = Q_i / C_{ox}$
- Solution?
  Cleaner fabrication environments, powerful chemical cleans, better wafers
- With simple C-V, we can learn and debug a great deal about the properties and quality of MOS caps:
  - Obtain oxide thickness from C in accumulation
  - Obtain substrate doping from C at V_t (HF)
  - Interface charge (Q_i) at V_{fb} from C-V across various oxide thicknesses!



Sources: E. Pop ECE 340 Lecture Slides

Influence of Material Parameters on Threshold Voltage

$$\Phi_{ms} = \Phi_m - \Phi_s$$

- In our ideal case, we found

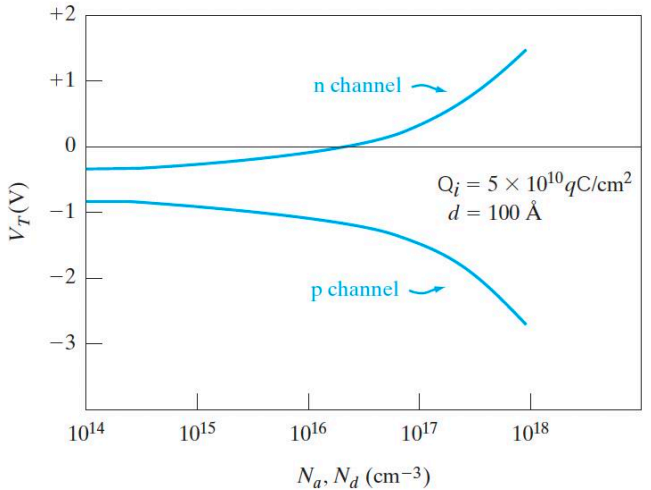
$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

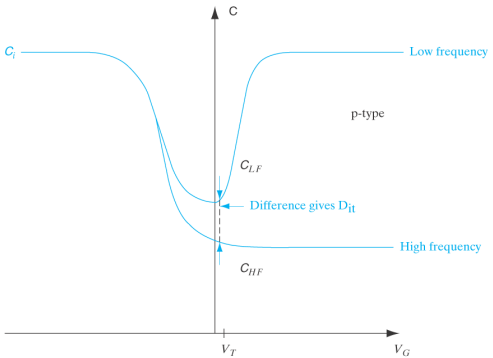
- In the non-ideal case, our threshold voltage must be modified to accommodate the ionic charge (traps): $V_t = \Phi_{ms} - \frac{Q_i}{C_{ox}} - \frac{Q_{dep}}{C_{ox}} + 2\Phi_F$

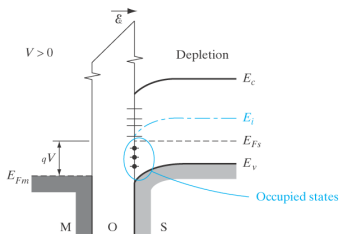
(a)

$V_T =$	Φ_{ms}	$-\frac{Q_i}{C_i}$	$-\frac{Q_d}{C_i}$	$+ 2\phi_F$
	(−)	(−)	(+) n channel (−) p channel	(+) n channel (−) p channel

(b)





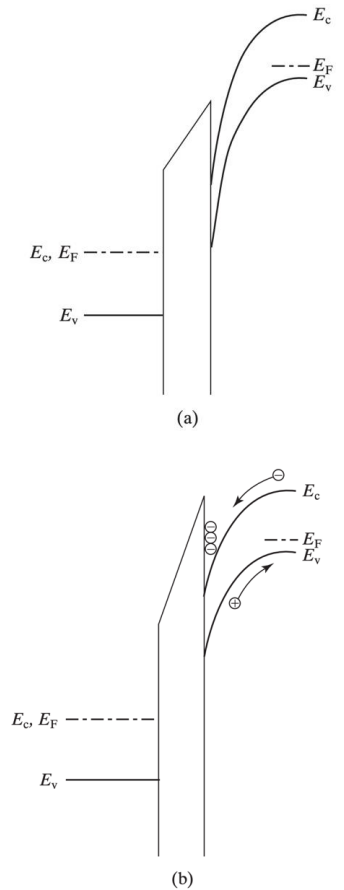


Sources: Textbook, E. Pop ECE 340 Lecture Slides

Application: CCD Imager

- MOS caps rarely used stand alone *except* for _____
- _____! Imager = sensing device that converts optical image into _____
- Large # of MOS caps are packed into a 2D _____
- nMOS: Immediately after we apply $V_g > V_t$, there are no e- on surface yet (no _____). Thermal generation is slow!
- The bands bend beyond $2\Phi_B$ and W_d__$W_{d,max}$ for a fraction of a second. This is called _____.
- If light shines on the MOS cap for these tens of ms, # of photo-generated e- collected at interface is proportional to _____.
- We have now converted an image (2D pattern of light intensity) into packets of e- stored in a 2D array of MOS caps!

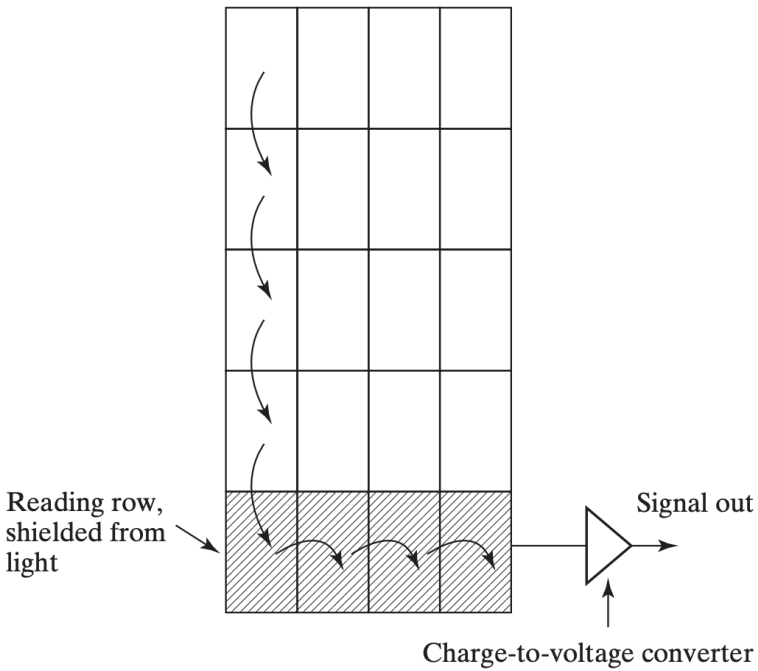
Deep depletion (a) immediately after $V_g > V_t$ applied, no e- at surface yet. (b) After exposure to light, photo-generated e- collect at surface.



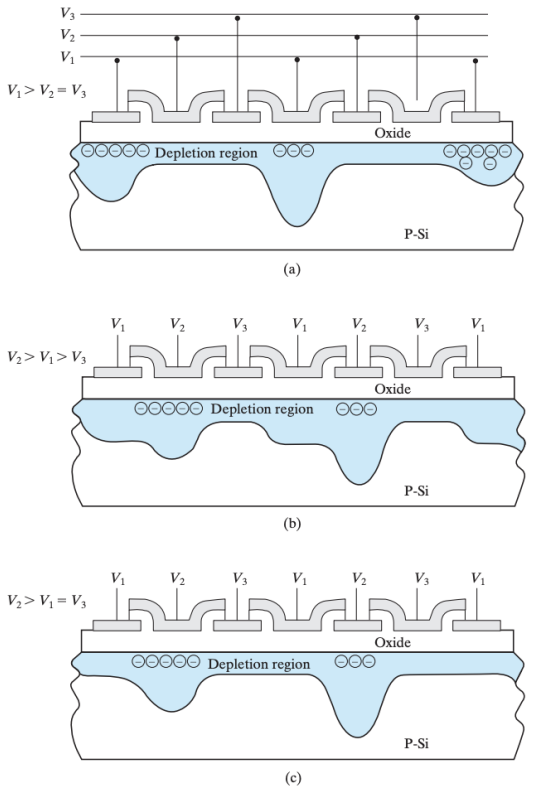
Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Application: CCD Imager

- How do we transfer these collected ”charge packets” to the edge of the array so they can be read into charge sensing _____?



Portion of a row in array is biased in the sequence (a), (b), (c), etc. The charge packets in (c) are shifted to the right by one capacitor compared to (a)



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